AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

1.   (Original) A method for storing bits of an ECC word in non-adjacent storage locations in a memory array of a memory device, the method comprising:

(a)   providing a memory device comprising a register and a memory array coupled with the register;

(b)   storing an ECC word in the register in a first direction;

(c)   reading the ECC word from the register in a second direction; and

(d)   storing bits of the ECC word in non-adjacent storage locations in the memory array.

2.   (Original) The invention of Claim 1, wherein the first direction is orthogonal to the second direction.

3.   (Original) The invention of Claim 1, wherein the memory array comprises a plurality of sub-arrays, and wherein the register comprises a plurality of sub-registers, each sub-register being associated with a respective sub-array.

4.   (Original) The invention of Claim 1, wherein adjacent bits of the ECC word are separated by 64 storage locations in the memory array.

5.   (Original) The invention of Claim 1, wherein the memory array comprises a plurality of write-once memory cells.

6.   (Original) The invention of Claim 1, wherein the memory array comprises a three-dimensional array of memory cells.

7.   (Original) The invention of Claim 1, wherein the memory array comprises a semiconductor material.

8.   (Currently Amended) A method for storing bits in non-adjacent storage locations in a memory array of a memory device, the method comprising:

   (a)   providing a memory device comprising a register and a memory array coupled with the register;

   (b)   providing a plurality of bits to the memory device;

   (c)   storing the plurality of bits in the register in a first direction;

   (d)   reading the plurality of bits from the register in a second direction, wherein an order in which the plurality of bits are read from the register is different from an order in which the plurality of bits are stored in the register, whereby bits that are adjacent to one another when provided to the memory device are not adjacent to one another when read from the register; and

(e)   storing the plurality of bits in the memory array, wherein bits that are adjacent to one another when provided to the memory device are stored in non-adjacent storage locations in the memory array.

9.   (Original) The invention of Claim 8, wherein the plurality of bits comprises bits of an ECC word.

10.   (Original) The invention of Claim 8, wherein the first direction is orthogonal to the second direction.

11.   (Original) The invention of Claim 8 further comprising:

(f)   reading the plurality of bits stored in (e) from the memory array;

(g)   storing the plurality of bits read in (f) in the register in the second direction; and

(h)   reading the plurality of bits stored in (g) from the register in the first direction.

12.   (Original) The invention of Claim 8, wherein the memory array comprises a plurality of sub-arrays, and wherein the register comprises a plurality of sub-registers, each sub-register being associated with a respective sub-array.

13.   (Original) The invention of Claim 8, wherein bits that are adjacent to one another when provided to the memory device are separated by 64 storage locations in the memory array.

14.   (Original) The invention of Claim 8, wherein the memory array comprises a plurality of write-once memory cells.

15.   (Original) The invention of Claim 8, wherein the memory array comprises a three-dimensional array of memory cells.

16.   (Original) The invention of Claim 8, wherein the memory array comprises a semiconductor material.

17.   (Original) A memory device comprising:

a memory array; and

a register coupled with the memory array, the register comprising:

a first set of wordlines and bitlines; and

a second set of wordlines and bitlines orthogonal to the first set of wordlines and

bitlines.

18.   (Original) The invention of Claim 17, wherein the first set of wordlines and bitlines is operative to store bits received by the memory device, and wherein the second set of wordlines and bitlines is operative to read bits that are to be stored in the memory array.

19.   (Original) The invention of Claim 18, wherein the first set of wordlines and bitlines is further operative to read bits that are to be outputted from the memory device, and wherein the

second set of wordlines and bitlines is further operative to store bits that are received from the memory array.

20.   (Original) The invention of Claim 17, wherein the memory array comprises a plurality of sub-arrays, and wherein the register comprises a plurality of sub-registers, each sub-register being associated with a respective one of the plurality of sub-arrays.

21.   (Original) The invention of Claim 17, wherein the memory array comprises a plurality of write-once memory cells.

22.   (Original) The invention of Claim 17, wherein the memory array comprises a three-dimensional array of memory cells.

23.   (Original) The invention of Claim 17, wherein the memory array comprises a semiconductor material.

24.   (Original) A method for storing bits in non-adjacent storage locations in a memory array of a memory device, the method comprising:

(a)   providing a memory device comprising a memory array, a column decoder, and a row decoder;

(b)   providing a plurality of bits to the memory device; and

(c) with at least one of the column decoder and row decoder, storing the plurality of bits in the memory array such that bits that are adjacent to one another when provided to the memory device are stored in non-adjacent storage locations in the memory array.

25. (Original) The invention of Claim 24, wherein the plurality of bits comprises bits of an ECC word.

26. (Original) The invention of Claim 24, wherein the memory array comprises a plurality of sub-arrays, and wherein the memory device comprises a plurality of column decoders and row decoders.

27. (Original) The invention of Claim 24, wherein the memory array comprises a plurality of write-once memory cells.

28. (Original) The invention of Claim 24, wherein the memory array comprises a three-dimensional array of memory cells.

29. (Original) The invention of Claim 24, wherein the memory array comprises a semiconductor material.

30. (Currently Amended) A method for storing bits in non-adjacent storage locations in a memory array of a memory device, the method comprising:

(a)   providing a host device coupled with a memory device comprising a memory array;

(b)   ~~with the host device,~~ re-ordering a plurality of bits such that bits that are adjacent to one another before the re-ordering are not adjacent to one another after the re-ordering ~~providing a plurality of bits arranged adjacent to one another~~;

(c)   with the host device, providing the re-ordered plurality of bits to the memory device ~~such that the memory device will store adjacent bits of the plurality of bits in non-adjacent storage locations in the memory array~~; and

(d)   with the memory device, storing the re-ordered plurality of bits in the memory array in the same order as provided to the memory device by the host device.

31.   (Currently Amended) ~~The invention of Claim 30,~~ A method for storing bits in non-adjacent storage locations in a memory array of a memory device, the method comprising:

(a)   providing a host device coupled with a memory device comprising a memory array;

(b)   providing a plurality of bits arranged adjacent to one another; and

(c)   with the host device providing the plurality of bits to the memory device such that the memory device will store adjacent bits of the plurality of bits in non-adjacent storage locations in the memory array;

wherein the plurality of bits comprises bits of an ECC word.

32.   (Currently Amended) ~~The invention of Claim 30,~~ A method for storing bits in non-adjacent storage locations in a memory array of a memory device, the method comprising:

(a)   providing a host device coupled with a memory device comprising a memory array;

(b)   providing a plurality of bits arranged adjacent to one another; and

(c)   with the host device providing the plurality of bits to the memory device such that the memory device will store adjacent bits of the plurality of bits in non-adjacent storage locations in the memory array;

wherein the memory array comprises a plurality of write-once memory cells.

33.   (Currently Amended) ~~The invention of Claim 30,~~ A method for storing bits in non-adjacent storage locations in a memory array of a memory device, the method comprising:

(a)   providing a host device coupled with a memory device comprising a memory array;

(b)   providing a plurality of bits arranged adjacent to one another; and

(c)   with the host device providing the plurality of bits to the memory device such that the memory device will store adjacent bits of the plurality of bits in non-adjacent storage locations in the memory array;

wherein the memory array comprises a three-dimensional array of memory cells.

34.   (Currently Amended) ~~The invention of Claim 30,~~ A method for storing bits in non-adjacent storage locations in a memory array of a memory device, the method comprising:

(a)   providing a host device coupled with a memory device comprising a memory array;

(b)   providing a plurality of bits arranged adjacent to one another; and

(c)   with the host device providing the plurality of bits to the memory device such that the memory device will store adjacent bits of the plurality of bits in non-adjacent storage locations in the memory array;

wherein the memory array comprises a semiconductor material.